REMARKS

The objection to claims 4 - 6 and 13 - 15 and the indication that such claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, is acknowledged. However, applicants note that such claims have been retained in dependent form at this time.

By the present amendment, independent claims 1 and 9 have been amended to clarify the structural arrangement of the present invention and applicants submit that all claims patentably distinguish over the cited art, as will become clear from the following discussion.

The rejections of claims 1 - 2, 9 - 11 and 18 - 20 under 35 USC 102(b) as being anticipated by US 5,847,781 (Ono et al) and the rejection of claims 3, 7 - 8, 12 and 16 - 17 under 35 USC 103(a) as being unpatentable over Ono et al further in view of US 5,798,744 (Tanaka et al), such rejections are traversed insofar as they are applicable to the present claims and reconsideration and withdrawal of the rejections are respectfully requested.

As to the requirement to support a rejection under 35 USC 102, reference is made to the decision of In re Robertson, 49 USPQ 2d 1949 (Fed. Cir. 1999), wherein the court pointed out that anticipation under 35 U.S.C. §102 requires that each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. As noted by the court, if the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if the element is "inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Moreover, the court pointed out that inherency, however, may not be established by probabilities or

possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

With regard to the requirements to support a rejection under 35 USC 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court pointed out that the PTO has the burden under '103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Furthermore, such requirements have been clarified in the recent decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". The court pointed out:

> The Examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is immaterial to patentability, and could not be resolved on subjected belief and unknown authority. It is improper, in determining whether a person

> of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher."... Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion. (emphasis added)

Turning to claim 1 and figures 1 and 4 of the drawings of this application, in accordance with the present invention, a display device includes a display area in which a liquid crystal LC as shown in the left-hand portion of Figure 1 is contained between a substrate 1A and a 1B, and in which display area is provided various circuitry as shown in Fig. 2, for example, for effecting display. The display area is sealed by a sealing material 13 as shown in Fig. 1 and to the right side of the sealing material 13 and the liquid crystal LC is provided a peripheral area on the substrate 1A. As shown in Fig. 1, a signal line 2 is extended from the display area in the region of the liquid crystal LC to the peripheral area on the substrate 1A and, as illustrated, a first insulating film 4, a semiconductor layer 6 and a second insulating film in the form of the protecting film 9 in such order covers or is disposed over the signal line 2 at the peripheral area. Such features are clearly set forth in independent claims 1 and 9 as amended, as well as unamended claim 18 of this application. That is, claim 1 recites "wherein a signal line is extended from said display area to said peripheral area on said substrate, and a first insulating film, a semiconductor layer and a second insulating film in this order covers or are provided over said signal line at said peripheral area". (emphasis added) Claim 9 recites "a first insulating film, a semiconductor layer and a second insulating film are formed on or over said signal line at said peripheral area" (emphasis added) while claim 18 recites "a first insulating film, a semiconductor layer, and a second insulating film, are formed at a peripheral area of said substrate; and a signal line formed under said first insulating film, said semiconductor layer and said second insulating film".

(emphasis added). Applicants submit that such features are not disclosed or taught in the cited art irrespective of the contentions by the Examiner.

Turning to Ono et al, the Examine refers to Figures 2 - 7 thereof and contends that the structure as illustrated corresponds to the claimed features of this application. Applicants submit that the Examiner's position is erroneous and Ono et al does not disclose a display device with a display area and a peripheral area having the features as claimed, as will become clear from the following discussion.

As to claims 1 and 2:

FIG.4 in Ono el al (USP 5,847,781) is a plan view showing a portion ranging from the vicinity of the end of the gate line GL to a gate terminal GTM to be connected to an external driver circuit on the TFT substrate TFTSUB. And FIG.5 in Ono et al is a sectional view taken on line V-V of FIG.4.

FIG. 4 Ono et al. (USP.5847781)

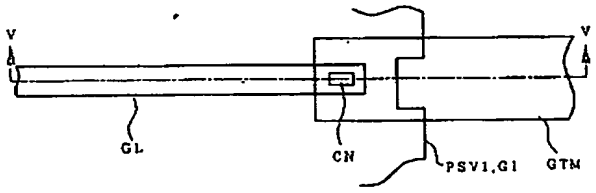


FIG. 5 Ono et al. (USP.5847781)

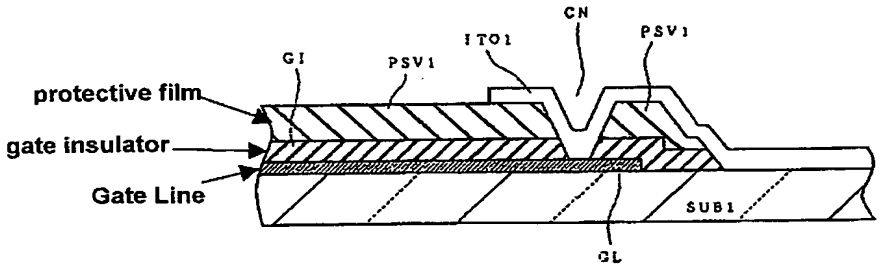


FIG.5 in Ono et al discloses a gate insulator and a protective film covered on a Gate Line CL. FIG.5 in Ono et al fails to disclose a first insulating film, a semiconductor layer, and a second insulating film in this order covers or are provided over said signal line at said peripheral area.

FIG.6 in Ono et al is a plan view showing a portion ranging from the vicinity of the end of the date line DL to a drain terminal DTM to be connected to an external driver circuit on the TFT substrate. And FIG.7 in Ono et al is a sectional view taken on line.

FIG. 6 Ono et al. (USP.5,847,781)

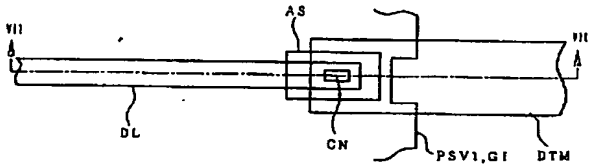


FIG. 7 Ono et al. (USP.5,847,781)

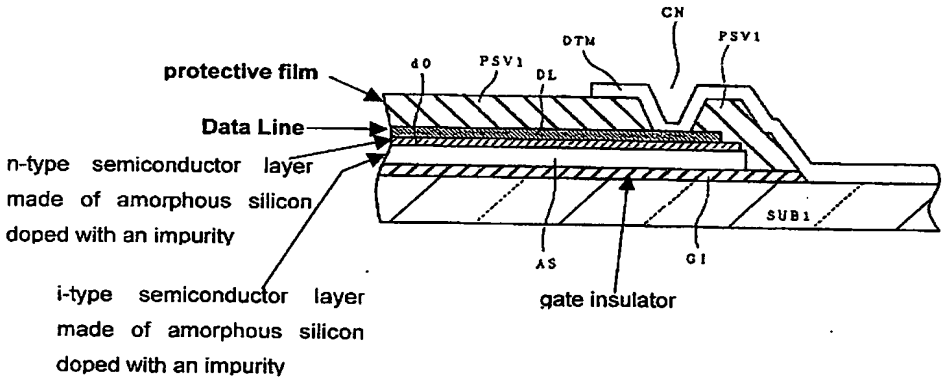
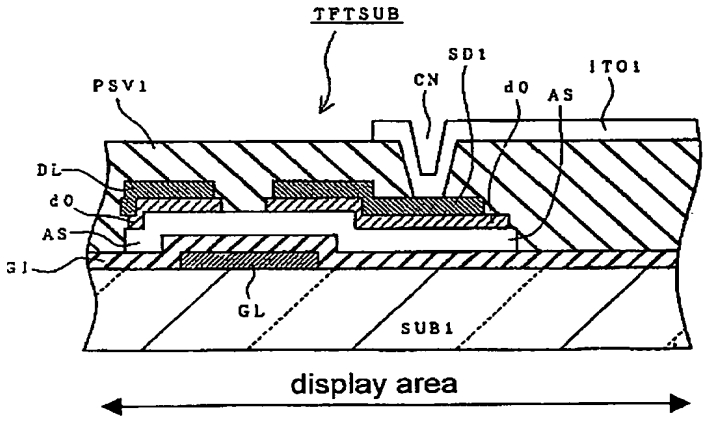


FIG.7 in Ono et al only discloses a protective film covered on a Data Line DL and n-type semiconductor layer, i-type semiconductor layer and a gate insulator formed under a Data Line. FIG.7 in Ono et al fails to disclose a first insulating film, a semiconductor layer, and a second insulating film in this order covers or are provided over said signal line at said peripheral area.

FIG. 3 in Ono et al merely discloses that the gate insulating film, the semiconductor layer, and the protective insulating film are formed at the TFT region in the display area. FIG.3 in Ono et al fails to disclose a first insulating film, a semiconductor layer, and a second insulating film in this order covers on or are provided over said signal line at said peripheral area.

FIG. 3 Ono et al. (USP.5,847,781)



Applicants submit that it is apparent from the above discussion that irrespective of the Examiner's position, Ono et al fails to disclose or teach in the sense of 35 USC 102 or 35 USC 103 the recited features of claim 1 and the

dependent claims thereof such that all claims should be considered allowable at this time.

As to Claims 9 - 11:

FIG.5 in Ono et al fails to disclose a first insulating film, a semiconductor layer, and a second insulating film are formed on or over said signal line at said peripheral area, as recited in claim 9. FIG.7 in Ono et al fails to disclose a first insulating film, a semiconductor layer, and a second insulating film are formed on or over said signal line at said peripheral area.

Accordingly applicants submit that Ono et al does not disclose or teach the recited features of claim 9 and the dependent claims in the sense of 35 USC 102 or 103 and all claims patentably distinguish over the cited art and should be considered allowable.

As to Claims 18 - 20:

FIG.5 in Ono et al fails to disclose a signal line formed under said first insulating film, said semiconductor layer, and said second insulating film at a peripheral area of said substrate, as recited in claim 18 and the dependent claims. Furthermore, FIG. 7 in Ono et al fails to disclose a signal line formed under said first insulating film, said semiconductor layer, and said second insulating film at a peripheral area of said substrate.

Accordingly, applicants submit that claim 18 and the dependent claims patentably distinguish over the cited art in the sense of 35 USC 102 and 103 and all claims should be considered allowable.

As to Claims 3,7, and 8:

As to the rejection of the claims under 35 USC 103, Tanaka et al (USP 5,798,744) merely discloses that the driver IC is mounted on the peripheral area, and the output terminal of the driver is connected to the terminal of the image signal line, that is one end of the signal line is connected to an output terminal of the driver IC. However, Tanaka et al fails to disclose a first insulating film, a semiconductor layer, and a second insulating film in this order covers or are provided over said signal line at said peripheral area, as recited in claim 1, which features are also not disclosed or taught by Ono et al. Thus, Tanaka et al fails to overcome the deficiencies of Ono et al, as pointed out above, and the combination fails to provide the claimed features. See, In re Fine, supra. Thus, the claims should also be considered allowable.

Tanaka et al. (USP.5,798,744)

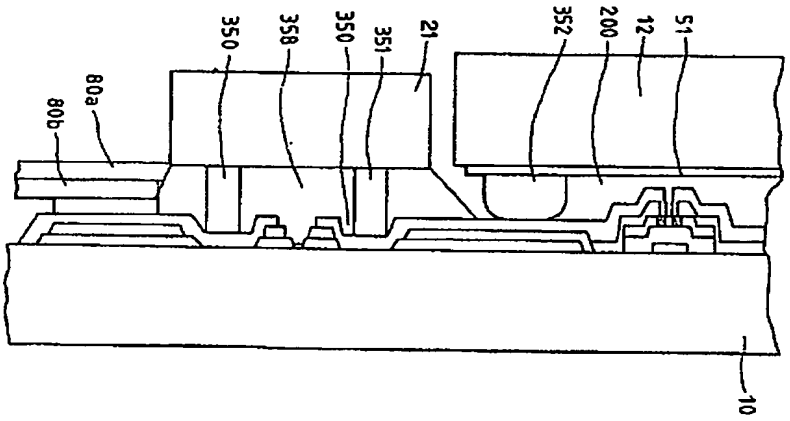


FIG. 7

As to Claim 12, 16, and 17:

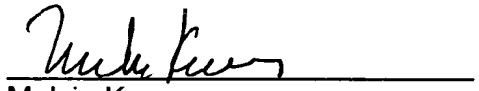
Hereagain, Tanaka et al fails to overcome the deficiencies of Ono et al in that Tanaka et al like Ono et al fails to disclose a first insulating film, a semiconductor

layer, and a second insulating film are formed on or over said signal line at said peripheral area, as recited in claim 9 and the dependent claims. Thus, applicants submit that the combination fails to provide the claimed features in the sense of 35 USC 103 and all claims should be considered allowable.

In view of the above amendments and remarks, applicants submit that all claims should now be in condition for allowance and issuance of an action of a favorable nature is requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.38380CX1) and please credit any excess fees to such deposit account.

Respectfully submitted,



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